What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An integrated circuit memory device comprising:

a substrate assembly;

first, second, and third layers of metalization, each layer disposed in substantially parallel spaced relation over said substrate assembly and each including a plurality of traces;

a first plurality of I/O traces and a second plurality of non-I/O traces disposed among said traces of one of said layers, at least one non-I/O trace being disposed between two of said I/O traces.

2. A device as in claim 1 wherein said I/O traces and non-I/O traces are further arranged such that at least one I/O trace is disposed between two non-I/O traces.

3. An integrated circuit memory device comprising:

a substrate assembly;

first, second, and third layers of metalization, each layer disposed in substantially parallel spaced relation over said substrate assembly and each including a plurality of traces;

a first plurality of I/O traces and a second plurality of non-I/O traces disposed among said traces of one of said layers, at least one non-I/O trace being disposed between two of said I/O traces;

first and second circuit portions, said first circuit portion operatively connected to one of said I/O lines, said second circuit portion operatively connected to one of said non-I/O lines;

said first and second circuit portions adapted to apply first and a second signals to said I/O line and said non-I/O line respectively, such that said first signal transitions at a first time and said second signal transitions at a second, later, time, said first and second times staggered so as not to overlap.

4. An integrated circuit memory device comprising:

a substrate assembly, said substrate assembly including a plurality of memory arrays, said memory arrays each including a plurality of memory blocks; and

first, second, and third layers of metalization, wherein one of said layers includes at least one I/O line that is continuous within said one layer over a span of two or more memory blocks.

5. A device, as in claim 4, wherein a memory array includes at least four memory blocks, and wherein said at least one I/O line is continuous within said one layer over a span of said at least four memory blocks.

6. A device, as in claim 4, wherein a memory array includes at least eight memory blocks, and wherein said at least one I/O line is continuous within said one layer over a span of said at least eight memory blocks.

7. An integrated circuit memory device comprising:

a substrate assembly including a memory array;

said memory array including a plurality of memory blocks, at least eight of said memory blocks being arranged in spaced relation to one another in a first direction relative to said substrate assembly;

a sense amplifier stripe having a longitudinal axis oriented substantially parallel to said first direction;

first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly; and

an I/O trace disposed among said traces of one of said layers having a longitudinal axis oriented substantially parallel to said first direction.

8. A device as in claim 7 wherein said I/O trace spans at least four of said eight memory blocks.

9. A device as in claim 7 wherein said I/O trace spans at least eight of said memory blocks.

10. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly, wherein said third layer of metallic traces includes a plurality of I/O traces and a portion of a column select line;

said substrate assembly including a phase driver circuit within a gap cell region thereof.

11. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly, wherein said third layer of metallic traces includes a plurality of I/O traces and a portion of a column select line;

a further portion of said column select line disposed in said second layer of traces in proximity to, and substantially orthogonal to, each of said I/O traces.

12. A device as in claim 11 wherein said substrate assembly further comprises a phase driver circuit within a gap cell region thereof.

13. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly, wherein said third layer of metallic traces includes a plurality of I/O traces and a portion of a column select line;

a plurality of digit traces disposed among said first layer of metallic traces; said digit traces being in proximity to and substantially parallel to said portion of a column select line;

a further plurality of traces disposed among said second layer of traces; each trace of said further plurality of traces having a portion disposed in proximity to and substantially orthogonal to each digit line of said plurality of digit lines and to said column select line.

14. A device as in claim 13 wherein said substrate assembly further comprises a phase driver circuit within a gap cell region thereof.

15. An integrated circuit memory device comprising:

a substrate assembly;

a layer of metallic traces including a local phase line trace;

a pair of wordline driver circuits, each of said circuits including one transistor of a pair of transistors formed within a common active region of said substrate assembly, said transistors sharing a common drain, said drain having a single connection to said local phase line trace.

16. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

a global bleeder circuit disposed within said substrate assembly and adapted to supply a standby voltage; and

a sense amplifier circuit disposed within said substrate assembly;

a global bleeder trace, at least a portion of which is disposed among said traces of said third layer of traces, operatively connected to both said bleeder circuit and said sense amplifier, and adapted to communicate said standby voltage from said bleeder circuit to said sense amplifier.

17. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly, wherein

said third layer of metallic traces includes a plurality of I/O traces and a portion of a column select line;

first and second memory arrays disposed within said substrate assembly and coupled to said I/O traces and portion of said column select line;

said memory arrays in spaced relation to one another and defining a throat region of said substrate assembly therebetween; and

a row decoder circuit disposed within said throat region.

18. A device as in claim 17 wherein said memory integrated circuit further comprises:

at least one global wordline trace having a first portion disposed among said third layer of traces above said first memory array and a second portion disposed among said third layer of traces above said second memory array, said global wordline trace operatively connected to said row decoder.

19. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

a first portion of a power bus trace disposed among said third layer of traces;

a second portion of a power bus trace disposed among said second layer of traces, said second portion disposed in proximity to and substantially parallel to said first portion; and

a plurality of vias operatively connected between said first and second portions so as to provide an electrical connection therebetween.

20. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

a first portion of a ground bus trace disposed among said third layer of traces;

a second portion of a ground bus trace disposed among said second layer of traces, said second portion disposed in proximity to and substantially parallel to said first portion; and

a plurality of vias operatively connected between said first and second portions so as to provide an electrical connection therebetween.

21. An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

a sense amplifier stripe having a longitudinal axis in a first direction; a wordline driver stripe having a longitudinal axis in a second direction; and

a metallic trace disposed among said second layer of traces having a first portion with a longitudinal axis disposed parallel to said first direction and a second portion having a longitudinal axis disposed parallel to said second direction.

22. An integrated circuit memory device comprising:

a substrate assembly;

first, second, and third layers of metalization disposed in spaced relation over said substrate assembly, said first second and third layers arranged in proximal, intermediate, and distal relationship to said subassembly respectively;

a sense amplifier portion including a plurality of components having active regions disposed within said substrate assembly arranged substantially symmetrically about a plane orthogonal to said subassembly; and

said first layer being free of I/O traces in a region above said sense amplifier.

23. An integrated circuit memory device comprising:

a substrate assembly containing a plurality of electronic devices;

first second and third conductive layers, each layer including a plurality of conductive traces;

said conductive traces including a plurality of I/O lines disposed substantially within said third layer of said conductor portion;

said conductive traces including at least one column select trace; said column select trace including a first portion disposed within said third layer, and a second portion disposed within said second layer, said first and second column select trace portions connected to one another by at least one via;

said second portion of said column select trace disposed between said plurality of I/O lines and said substrate assembly.

24. An integrated circuit memory device comprising:

first, second, and third metalization layers provided over a substrate, each layer disposed in spaced relation to said substrate and to each other; said first second and third layers being arranged in proximal, intermediate, and distal relationship to said substrate respectively;

said third layer including a portion of a column select line;

said first layer including a digit line;

said digit line being substantially adjacent said column select line and substantially parallel thereto;

said second layer including a plurality of traces substantially orthogonal to an axis of said column select line and between said column select line and said digit line.

25. An integrated circuit memory device comprising:

two adjacent wordline driver circuits;

an active area having first and second transistors formed therein;

a portion of said active area including a doped region common to said two transistors;

one of said transistors being operatively connected to said first wordline driver circuit and the other of said transistors being operatively connected to said second wordline driver circuit.

26. A device as in claim 25 further comprising a local phase line including a point of connection operatively connected to said doped region.

27. An integrated circuit memory device comprising:

a substrate assembly;

a layer of metalization over a substrate, said layer including at least one global bleeder line;

a bleeder device disposed within said substrate having an output operatively connected to said bleeder line; and

a plurality of sense amplifiers disposed within said substrate each amplifier of said plurality being operatively connected to said bleeder line.

28. A device as in claim 27 further comprising:

a plurality of additional layers of metal traces;

said plurality of layers disposed between said global bleeder line and said substrate assembly.

29. A device as in claim 27 further comprising:

a memory array block;

said block disposed within said substrate assembly;

one of said plurality of sense amplifiers being disposed on one side of said block, and another of said plurality of sense amplifiers being disposed on a second opposite side of said block.

30. An integrated circuit memory device comprising:

a substrate assembly;

first and second memory arrays formed in said substrate assembly, said arrays disposed in spaced relation to one another and defining a throat therebetween;

a row decoder disposed in said substrate assembly within said throat;

a layer of metallic traces disposed in substantially parallel spaced relation over said substrate assembly; and

a global wordline trace disposed within said layer;

said global wordline trace being operatively connected to both said row driver and at least one of said arrays.

31. A device as in claim 30 further comprising:

at least one data read line and one data write line;

said lines being disposed adjacent said throat and within said layer of metallic traces.

32. An integrated circuit memory device comprising:

a substrate assembly having circuit structures fabricated thereon;

first, second, and third layers of metalization disposed in spaced relation above said substrate assembly, said first, second, and third layers being arranged in proximal intermediate and distal relationship to said substrate assembly respectively;

a first power trace disposed within said third metal layer; a second substantially parallel power trace disposed within said second layer; and

a plurality of vias disposed between and connecting said first and second traces to form a power bus.

33. A method of operating an integrated circuit memory device, said method comprising:

providing a layer of metalized traces including a plurality of I/O traces;

including within said layer a plurality of non-I/O traces, and disposing at least one non-I/O trace between two I/O traces;

introducing a first plurality of I/O signals, each exhibiting a transient portion and a non-transient portion, onto said plurality of I/O traces respectively;

introducing a second plurality of non-I/O signals, each exhibiting a transient portion and a non-transient portion, onto said plurality of non-I/O traces respectively, and applying said signals such that said I/O signal transient portions occur only during non-transient portions of said non-I/O signals.

34. A method of operating an integrated circuit as in claim 1, further comprising providing two additional layers of metalization, each closer to an underlying substrate than said I/O traces.

35. A method of operating an integrated circuit memory device comprising:

providing an integrated circuit including a substrate assembly and a layer of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

providing among said third layer of metallic traces a first plurality of I/O traces interspersed with a second plurality of non-I/O traces such that at least one non-I/O trace is disposed between any two of said I/O traces;

during a first time period, introducing a first plurality of electrical signals each including a transient portion followed by a non-transient portion, one onto each of said non-I/O traces respectively, and allowing each of said first plurality of signals to reach said non-transient portion;

during a second time period, subsequent to said first time period, introducing a second plurality of electrical signals, each including a transient portion followed by a non-transient portion, one onto each of said plurality of I/O traces respectively such that said transient portion of said second electrical signal occurs exclusively during said non-transient portion of said first electrical signal.

36. A method as in claim 35 further comprising a plurality of additional layers of metalization, wherein said plurality of I/O traces is spaced farther from said substrate than any of said additional layers.

37. A method of forming an integrated circuit memory device comprising:

forming a first layer of metallic traces over a substrate assembly which contains a plurality of sense amplifier portions;

forming a second layer of metallic traces over and insulated from said first layer of traces;

said second layer of traces including a first plurality of column select trace portions positioned over said sense amplifier portions;

forming a third layer of metallic traces over and insulated from said second layer of traces;

said third layer of traces including a plurality of I/O traces disposed above and substantially orthogonal to said column select traced portions; and

forming a further plurality of column select trace portions, which are substantially orthogonal to said I/O traces.

38. A method of forming an integrated circuit memory device, said method comprising:

forming first and second adjacent wordline driver circuits, each containing respective transistors;

forming said transistors within a common active region such that both share a doped region;

forming a phase line; and

operatively connecting said phase line to said doped region.

39. A method of forming an integrated circuit memory device comprising:

forming first, second, and third layers of metallic traces disposed above a substrate in spaced proximal, intermediate, and distal relation thereto respectively;

said first layer of traces including a plurality of digit lines;

said third layer of traces including a plurality of column select lines, said column select lines being disposed substantially parallel to said digit lines; and

said second layer of traces including a further plurality of traces disposed between said digit lines and said column select lines and substantially orthogonal to both said digit lines and said column select lines.

40. A method of forming an integrated circuit memory device comprising:

providing a substrate assembly;

providing a layer of metal traces disposed in substantially parallel spaced relation above said substrate assembly, said layer including a local phase trace;

providing an active region within said substrate assembly;

disposing first and second transistor gate assemblies in spaced relation above said active region, thereby defining first and second transistors; and

operatively connecting said local phase trace to said active region between said first and second gate assemblies, thereby operatively connecting said local phase trace to both said first and second transistors.

41. A method as in claim 40 further comprising:

providing a plurality of additional layers of metal traces; said plurality of layers disposed between said local phase trace and said substrate assembly.

42. A method of supplying a standby voltage to a sense amplifier of an integrated circuit memory device comprising:

providing a substrate assembly;

providing a layer of metallic traces disposed in substantially parallel spaced relation above said substrate assembly;

disposing within said layer of traces a global bleeder trace;

providing within said substrate assembly a bleeder circuit, said bleeder circuit being adapted to supply a standby voltage for a sense amplifier;

providing within said substrate assembly a plurality of sense amplifiers;

operatively connecting said global bleeder trace to said bleeder circuit;

operatively connecting said global bleeder trace to each sense amplifier of said plurality of sense amplifiers; and

operating said bleeder circuit and supplying said each sense amplifier with said standby voltage.

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~~44~~. A method of connecting a wordline in a memory integrated circuit comprising:

providing a substrate assembly including first and second memory arrays disposed in spaced relation to one another and defining a throat region therebetween;

providing within said throat region a row decoder circuit having a plurality of inputs and an output;

providing a plurality of address traces;

operatively connecting said plurality of address traces to said plurality of row decoder circuit inputs respectively;

providing first and second wordline driver circuits, each having an input and an output, within said first and second memory arrays respectively;

operatively connecting said output of said row decoder to said inputs of said first wordline driver circuit and to said input of said second wordline driver circuit; and

providing, within said first and second arrays respectively, first and second wordlines operatively connected to said respective outputs of said first and second wordline drivers.

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~~45~~. An integrated circuit memory device comprising:

a substrate assembly;

first, second, and third layers of metalization, each layer disposed in substantially parallel spaced relation over said substrate assembly and each including a plurality of traces;

a first plurality of column select traces and a second plurality of bleeder traces disposed among said traces of one of said layers, at least one bleeder trace being disposed between two of said column select traces.